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REMARKS and ARGUMENTS

Applicants appreciate the Examiners attention to this application. Claims 30-31 and claim 33 have been cancelled, while the other claims of 1-37 remain pending.

Claim Rejections -35 USC § 103(a)

The Office Action states:

3.   Claims 1- 3, 5-9, 11-13, 15, 18-22, 25- 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg et al. (Slipstream Execution Mode for CMP-Based Multiprocessors) herein referred to as Rotenberg, in view of Jamil (U.S. Patent Application Publication No. US 2003/0126365 A1).

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142.   It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

Applicant's claim 1 includes, "control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache associated with the second processor, the requested data to the first private data cache of the first processor." As stated by

the Office Action, Rotenberg does not disclose any logic to provide, or push as now amended, requested data into the first private data cache. Furthermore, note that in applicant's claim 1 the push of requested data into the **first private cache** is **responsive to a miss of the requested data...in the second private cache**. Essentially, a miss in the second cache causes the control logic to push the requested data to the first private cache associated with the first processor.

In contrast, Jamil only describes maintaining coherency (i.e. obtaining modified data from another dedicated cache) between dedicated caches without off-chip transfer (See Abstract); specifically, the on-chip transfer is in response to a normal coherency request for a cache line (see paragraph 0004 and Figure 2 block 210 – first processor requests data and block 240 request write-back). Therefore, the on-chip transfer of a modified cache line in Jamil is in response to a normal cache request with Jamil's intended advantage of transferring on-chip and not through an off-chip higher-level memory. In direct contrast, applicant's claim 1 includes a push of requested data to one processor in response to a miss in another processor.

Embodiments of pushing requested data may be seen in dependent claim 4 (the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to broadcast the requested data to an affinity group of processors including at least the first processor) and claim 5 (the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to unicast the requested data to the first processor). When the requested data is retrieved, in claim 4 it is broadcasted to an affinity group that includes the first processor, and in claim 5, the data is unicasted to the first processor. Note that neither Rotenberg or Jamil disclose broadcast or unicasting as in claims 4 and 5 in response to missing a second cache and retrieving the requested data.

Similarly, applicant's now independent claim 7 includes, "logic to retrieve data for the load instruction from a higher level memory and to provide the data to the first private cache associated with the first processor core in response to a miss to the second private cache responsive to execution of the load instruction in the second speculative thread with the second processor core." As stated above, Rotenberg does not disclose providing data to the first private cache in response to a miss to the second private cache. Similarly, Jamil discloses transferring a modified line from one dedicated cache to another dedicated cache, in response to a request for the line, but does not disclose providing data in response to a miss to the second private cache response to execution of the load instruction in the second speculative thread.

Applicant's claim 11 includes, "control logic to provide the requested data to the first data cache associated with the first processor in response to the retrieval logic retrieving the requested data and **without a request from the first processor**." As stated above, Rotenberg does not disclose providing requested data to a data cache associated with a first processor in response to a miss/retrieval of a second processor. In addition, Jamil disclose transferring a modified line, i.e. a line written to by another processor, and does not disclose logic to retrieve/provide requested data **to a first data cache** associated with a first processor in response to **a miss of requested data** for a delinquent **load instruction** in the second data cache.

Similarly, applicant's claim 18 includes, "prefetching load data for the load instruction into the first private cache responsive to missing the second private cache in response to executing the load instruction within the helper thread with the second core." As stated above, neither Rotenberg, which discusses prefetching through sharing a second level cache, or Jamil, which discusses transferring a modified cache line in response to a first processor request,

disclose prefetching load data into a first private cache response to missing a second private cache.

Applicant's claim 25 includes, "pushing, unsolicited from the main core, the load data into a main private cache of the main core in response to fetching the load data for the load instruction." As stated above, neither Jamil or Rotenberg disclose pushing load data to a main private cache in an unsolicited manner from the main core in response to fetching the load data, which is in response to a miss in a helper private cache of a helper core.

The Office Action also states:

> 17.   Claims 4, 16, and 32-37 are rejected under 35 U.S.C. 103(a) as being
> unpatentable over Rotenberg in view of Jamil and Jeddeloh (U.S. Patent No. US 6,789,
> 168 B2).

Applicant's claim 32 includes, "helper threading logic to push fill data to a first private cache of the first processor, the fill data to be prefetched by the second processor and to be pushed to the first private cache before a request for the fill data is issued by the first processor." Again, Rotenberg only discloses potential prefetch due to overlap of a separately executed reduced task, but that the prefetching only results in better locality than data residing in system memory, i.e. the prefetched data resides in a cache associated with the separately executed reduced task. Yet, Rotenberg does not disclose prefetching into a first private cache of the first processor by a second processor or that the data is to be so pushed before any request from the first processor. Additionally, Jamil discloses on-chip transfer in response to explicit coherence requests, which does not include pushing of data before a request for the fill data. Furthermore, Jeddeloh is only disclosed for a system memory including a DRAM, and also does not disclose the aforementioned elements of applicant's claim 32.

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Conclusion

Therefore, applicant respectfully submits that applicant's independent claims 1, 7, 11, 18, 25, and 32, as well as their dependent claims, are now in condition for allowance for at least the reasons stated above. If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
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